CLAIMS

What is claimed is:

[c1] 1. A method for manufacturing a nonvolatile memory capable of storing multi-bits binary information on a semiconductor substrate, said method comprising the steps of:

forming an oxide on said semiconductor substrate;

forming a conductive layer on said oxide layer;

patterning said conductive layer to form a gate structure to act as a control gate;

forming a first isolation layer over said gate structure;

forming a second isolation layer over said first isolation layer;

performing an etching to etch said second isolation layer and said first isolation layer, thereby forming a L-shape structure attached on sidewall of said gate structure and spacers on said L-shape structure, wherein said spacers functions as floating gates;

performing an ion implantation using said gate structure and said spacer as a mask to form a first and a second doped regions in said semiconductor substrate adjacent to said spacers, wherein a channel under said gate structure keeps a distance from said first and said second doped regions.

[c2] 2. The method of Claim 1, further comprising forming silicide material on said gate structure and said source and drain regions.

[c3] 3. The method of Claim 1, wherein said spacer is formed by an anisotropical etching.

[c4] 4. The method of Claim 1, wherein said first isolation layer includes SiO_2 or HfO_2.

[c5] 5. The method of Claim 1, wherein said second isolation layer includes nitride.

[c6] 6. The method of Claim 1, wherein said silicide material includes $TiSi_2$, $CoSi_2$ or NiSi.

[c7] 7. A nonvolatile memory capable of storing multi-bits binary information bits, comprising:

an oxide formed on a substrate;

a control gate formed on said oxide;

a L-shape structure attached on sidewall of said control gate, a vertical portion of said L-shape structure attaching on the side wall of said gate and a lateral portion where tunneling will be occurred is formed on said substrate;

spacers formed on said L-shape structure to act as a floating gate;

a first doped region and a second doped region formed in said substrate adjacent to said spacers, a first and a second fringing field induced channels under said first and said second spacers, wherein said first and a second fringing field induced channels located between the main gate-induced channel, said first and second doped regions sitting adjacent to said first and second fringing field induced channels, respectively;

wherein said spacers representing a first binary status by injecting and storing electrical charge in said spacers or to represent a second binary status by not injecting electrical charge into said spacer.

[c8] 8. The memory of Claim 7, further comprising silicide material formed on said control gate and said source and drain regions.

[c9] 9. The method of Claim 8, wherein said silicide material includes $TiSi_2$, $CoSi_2$ or NiSi.

[c10] 10. The method of Claim 7, wherein said L-shape structure includes SiO_2 or HfO_2.

[c11] 11. The method of Claim 7, wherein said spacer includes nitride.

[c12] 12. A method of programming a nonvolatile memory capable of storing multi-bits binary information bits, said memory cell having a plurality of doped regions with a channel and having a gate above said channel, a L-shape dielectric layer formed on side wall of said gate, spacers attached on said L-shape dielectric layer, said method comprising:

programming a first bit by applying programming voltages to a first doped region of said plurality of doped regions and to said gate while applying programming current or ground potential on a second doped region of plurality of doped regions, thereby injecting and storing electrical charge in a first spacer of said spacers adjacent to said first doped region to represent a first binary status, or to represent a second binary status by not injecting electrical charge into said first spacer.

[c13] 13. The method of Claim 12, further comprising:

programming a second bit by applying programming voltages to a second doped region of a plurality of doped regions and to said gate, applying said first doped region with programming current or ground potential, thereby injecting and storing electrical charge in a second

spacer of said spacers close to said second doped region to represent said first binary status, or to represent said second binary status by not injecting electrical charge into said second spacer.

[c14] 14. The method of Claim 13, further comprising:

programming a third bit by applying programming voltages to a third doped region of said plurality of doped regions and to said gate, applying a fourth doped region of said plurality of doped regions with programming current or ground potential, thereby injecting and storing electrical charge in a third spacer of said spacers close to said third doped region, or to represent said second binary status by not injecting electrical charge into said third spacer.

[c15] 15. The method of Claim 14, further comprising:

programming a fourth bit by applying programming voltages to said forth doped region of said plurality of doped regions and to said gate, applying said third doped region with programming current or ground potential, thereby injecting and storing electrical charge in a fourth spacer of said spacers close to said fourth doped region to present said first binary status, or to represent said second binary status by not injecting electrical charge into said fourth spacer.

[c16] 16. A method of erasing a nonvolatile memory capable of storing multi-bits binary information bits, said memory cell having a first doped region and a second doped region with a channel and having a gate above said channel, a L-shape dielectric layer formed on side wall of said gate, spacers attached on said L-shape dielectric layer, said method comprising:

erasing a first bit of said multi-bits binary information bits by applying erasing voltages to said gate and a first doped region such that to

cause charge representing a first binary status to be removed from a first spacer of said spacers for charge trapping.

[c17] 17. A method of Claim 16, further comprising:

erasing a second bit of said multi-bits binary information bits by applying erasing voltages to said gate and a second doped region such that to cause charge representing a second binary status to be removed from a second spacer of said spacers for charge trapping.

[c18] 18. A method of reading an nonvolatile memory capable of storing multi-bits binary information bits, said memory cell having a first doped region and a second doped region with a channel and having a gate above said channel, an L-shape dielectric layer formed on side wall of said gate, spacers attached on said L-shape dielectric layer, said method comprising:

applying a reading bias on said gate and a second doped region, said reading bias having levels lower than the voltages applied during programming for sensing a channel current to determine whether the channel current is significantly representing a first binary status in said spacer adjacent to said first doped region or said channel current is relative low to said significant channel current representing a second binary status in said spacer adjacent to said first doped region.

[c19] 19. A method of Claim 18, further comprising:

applying said reading bias on said gate and a first doped region, said reading bias having levels lower than said voltages applied during programming for sensing said channel current to determine whether the channel current is significantly representing said first binary status in said spacer adjacent to said second doped region or said channel current is relative low to said significant channel current

repressing said second binary status in said spacer adjacent to said second doped region.

[c20] 20. A method of erasing a nonvolatile memory capable of storing multi-bits binary information bits, said memory cell having a first doped region and a second doped region and having a gate above a channel, a L-shape dielectric layer formed on side wall of said gate, spacers attached on said L-shape dielectric layer, said method comprising:

erasing the binary state by removing charge from said first spacer by exposing said nonvolatile memory in UV environment; and

erasing the binary state by removing charge from said second spacer by exposing said nonvolatile memory in UV environment.